REMARKS

Claims 1-26 were pending. All stand rejected. The Applicant hereby requests further consideration and re-examination in view of the amendments above and remarks set forth below.

Objection to the Drawings:

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) for the reason that they do not include the reference numeral "345" mentioned in the description. The Examiner stated that corrected drawing sheets were required in reply to the office action.

The Applicant has amended the description at page 9, lines 19-26 and page 11, lines 20-23 to replace the reference numeral "345" with the reference numeral "350." The reference numeral "350" is shown in the drawings in Figure 3. Therefore, the present application is now in compliance with 37 CFR 1.84(p)(5), which requires that reference characters not mentioned in the description not appear in the drawings and that reference characters mentioned in the description appear in the drawings. Thus, the Applicant respectfully submits that corrected drawings are not required in order to comply with 37 CFR 1.84(p)(5). The Applicant requests that the objection be removed in view of the above amendments to the description.

The Applicant also amended the paragraph at page 9, lines 19-26, to correct a typographical error. In particular, the Applicant replaced "maybe" with "may be."

Rejections under 35 U.S.C. § 103:

Claims 1-26 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application. Ser. No. 09/771,963 (hereinafter, "Bowen") in view of U.S. Patent No. 6,662,302 (hereinafter, "Garey").

Regarding claim 1, the Examiner stated that Bowen teaches parsing a source code at paragraph [0113], performing a plurality of optimizations on the parsed code at paragraph [0113], and generating a configuration instruction set based on the optimized source code at paragraph [0298] and at Figure 11. The Examiner further stated that Bowen does not teach automatically selecting one of the generated configuration instruction sets according to user-defined criteria. However, the Examiner stated that Garey teaches automatically selecting one of the plurality of generated configuration instruction sets based on user-defined criteria, the selected

configuration instruction set being used to configure hardware at column 3, lines 32-45. The Examiner further stated that the alternative logic configuration is chosen in response to the input data, the input data being viewed by the Examiner as the user criteria. The Examiner stated that it would have been obvious to combine the teachings of Bowen and Garey "to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data [Column 1, lines 40-42]."

The Applicant respectfully traverses the rejection. As explained more fully below, the Applicant submits that it would not have been obvious to combine the Bowen and Garey references in the manner suggested by the Examiner and, even if combined, the Applicant submits that such a combination would not include all of the limitations of the Applicant's claimed invention.

The Applicant's invention is directed toward a method and apparatus for compiling source code to configure hardware. Title, Applicant's specification. The source code typically includes programming statements that are created by a programmer and which represent functional units or computations, such as routines, sub-routines, or other computational statements. Applicant's specification at page 6, lines 7-17. The source code is input to a hardware compiler which compiles the source codes into configuration instruction sets. Applicant's specification at page 6, lines 19-21. This includes the complier parsing the source code. Applicant's specification at page 7, lines 8-10 and 18-28. Optimization processes performed by the compiler generate a plurality of the configuration sets. Applicant's specification at page 8, lines 2-3. One of the plurality of configuration sets is then selected based on user-defined criteria. Applicant's specification at page 8, lines 20-21. A hardware realization is generated using the selected configuration instruction set. Applicant's specification at page 9, lines 8-9.

Thus, the Applicant's claim 1 recites a method of compiling comprising parsing a source code, performing a plurality of optimizations on the parsed code, performing a plurality of optimizations on the parsed code, generating a plurality of configuration instruction sets based on the optimized source code, and automatically selecting one of the plurality of generated configuration instruction sets according to user-defined criteria, the selected configuration set being used to configure hardware.

Regarding the Bowen reference, it is directed to a co-design system whose target is an electronic circuit that includes both dedicated hardware and software

controlled resources. Bowen, at para. [0040]. In describing the problem to be solved by Bowen, it explains that system designers face the problem of deciding which functions are to be performed in hardware and which functions are to be performed in software. Bowen at para. [0008]. Bowen refers to this as "partitioning" the design. Bowen at para. [0008]. Therefore, the hardware/software co-design system of Bowen includes a partitioning means that decides the partitioning to obtain an optimal partitioning and optimal size of hardware and processor to run the software. Bowen at para. [0027].

The co-design system of Bowen receives a behavioral description of the target electronic system and automatically partitions the required functionality between hardware and software, while being able to vary the parameters (e.g. size or power) of the hardware and/or software. Bowen, at para. [0040]. The co-design system outputs a description of the required processor (which can be in the form of a net list for placement on an FPGA), machine code to run on the processor, and a net list or register transfer level description of the necessary hardware. Bowen, at para. [0040]. The automatic partitioning can be performed by using an optimization algorithm, e.g. a genetic algorithm, which generates a partitioning based on estimates of performance. Bowen, at para. [0040].

A partitioner 208 (Figure 2) of Bowen generates a control/data-flow graph and groups parts of the description into blocks, referred to by Bowen as "partitioning blocks," which are indivisible by the partitioner. Bowen at para. [0116]. The genetic algorithm is used to optimize the partitioning. Bowen at para. [0032].

Regarding the Garey reference, it is directed toward a signal processor. Garey, Abstract. Garey explains that the problem it is intended to solve is that conventional systems that perform data processing do not possess the ability to adapt to various data types on which the data processor must operate. Garey at col. 1, lines 17-19. Garey also explains that conventional hardware signal processors typically provide limited functionality in that they are unable to perform a substantially wide variety of operations to accommodate various pluralities of input data. Garey at col. 1, lines 33-42.

Garey proposes a solution to this problem by a signal processor having programmable logic circuitry that operates on a plurality of data. Garey at col. 1, lines 54-56. The programmable logic circuitry is re-configurable in response to a plurality of parameters including characteristics of a plurality of input data that is

provided to the signal processor. Garey, Abstract. Programmable logic configuration circuitry 130 (Figure 1) selects a predetermined logic configuration from among a predetermined plurality of default logic configurations contained within default configuration circuitry 132 (Figure 1). Garey at col. 3, lines 31-35. Adaptive configuration circuitry 134 (Figure 1) selects an alternative logic configuration in response to a number of factors including, among other things, a plurality of input data that is provided to the signal processor. Garey at col. 3, lines 42-45.

Thus, Garey is directed to a signal processing hardware circuit that is provided with multiple selectable configuration options so that it is able to perform a wide variety of operations to accommodate various input data. In contrast, Bowen is directed to aiding a designer of a combined hardware and software system in optimally determining partitioning between the hardware and the software in such a combined system. Accordingly, Bowen and Garey are directed toward completely different problems encountered in completely different types of systems. Each provides a solution to address a particular problem encountered in the distinct system type to which it pertains. Therefore, it would not have been obvious to combine the references because there would not have been a motivation to make a combination of these different solutions to problems encountered in these different system types. For at least this reason, claims 1-26, which were rejected in view of the combination of Bowen and Garey, are allowable.

Further, as mentioned above, the Examiner stated that it would have been obvious to combine the teachings of Bowen and Garey to obtain a circuit which can perform a wide variety of operations to accommodate various pluralities of input data. However, this motivation suggested by Examiner is purported to be achieved by Garey alone. This is because Garey states that it provides a solution the problem of conventional hardware signal processors typically providing only limited functionality and being unable to perform a substantially wide variety of operations to accommodate various input data. See Garey at col. 1, lines 33-42 and col. 2, lines 53-55. Accordingly, this rationale cannot provide a motivation to make the combination of Garey with Bowen. This because Garey alone already achieves this stated goal and, thus, the addition of features from Bowen would be unnecessary to achieve the goal. This is another reason why claims 1-26 are allowable.

Morever, even if combined, a combination of Bowen with Garey would not achieve the Applicant's claimed invention. As explained above, claim 1 requires

generating a plurality of configuration instruction sets based on the optimized source code and automatically selecting one of the plurality of generated configuration sets according to a user-defined criteria, the selected configuration instruction set being used to configure the hardware. This is a significant feature of the Applicant's invention because it provides a novel and non-obvious way for helping to ensure that design criteria are met.

However, Bowen does not suggest or disclose generating a plurality of configuration instruction sets based on optimized source code. Regarding this claim feature, the Examiner stated that Bowen teaches generating "a configuration instruction set" at paragraph [0298] of Bowen. Therefore, at most, Bowen discloses generating one configuration instruction set, whereas, the Applicant's claim 1 requires generating a plurality of instruction sets based on the optimized source code and then selecting one instruction set from among the plurality. Garey does not suggest or disclose this feature either. While the programmable logic configuration circuitry of Garey selects a predetermined logic configuration from among a predetermined plurality of default logic configurations contained within the default configuration circuitry, Garey does not teach or suggest generating a plurality configuration instruction sets based on optimized source code, as is required by the Applicant's claim 1.

This is another reason why the Applicant's claim 1 is allowable over the Bowen and Garey references, taken singly or combination. This is also another reason why the Applicant's claims 2-10 are allowable, being dependent upon an allowable base claim 1.

The Applicant's claim 10 recites automatically generating a plurality of configuration instruction sets based on optimized source code and automatically selecting one of the plurality of generated configuration instruction sets according to a user-defined criteria, the selected configuration instruction set being used to configure hardware. As explained above regarding claim 1, Bowen and Garey, taken singly or in combination, do not suggest or disclosure such a feature. Therefore, this is another reason why claim 11 is allowable. This is also another reason why claims 12-16 are allowable, being dependent upon an allowable base claim 11.

The Applicant's claim 17 recites a compiler for automatically generating a plurality of configuration sets from source code and selecting one of the plurality of configuration sets based on user-defined criteria. As explained above regarding claim

1, Bowen and Garey, taken singly or in combination, do not suggest or disclosure such a feature. Therefore, this is another reason why claim 17 is allowable. This is also another reason why claims 18-22 are allowable, being dependent upon an allowable base claim 17.

The Applicant's claim 23 recites means for generating a plurality of configuration sets from source code and means for automatically selecting one of the plurality of generated configuration instruction sets according to a user-defined criteria. As explained above regarding claim 1, Bowen and Garey, taken singly or in combination, do not suggest or disclosure such a feature. Therefore, this is another reason why claim 23 is allowable. This is also another reason why claims 24-26 are allowable, being dependent upon an allowable base claim 23.

Conclusion:

In view of the above, the Applicant submits that all of the pending claims are now allowable. Allowance at an early date would be greatly appreciated. Should any outstanding issues remain, the Examiner is encouraged to contact the undersigned at (408) 293-9000 so that any such issues can be expeditiously resolved.

Respectfully Submitted,

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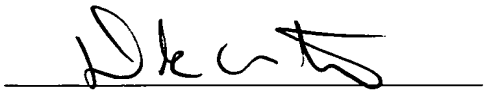

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